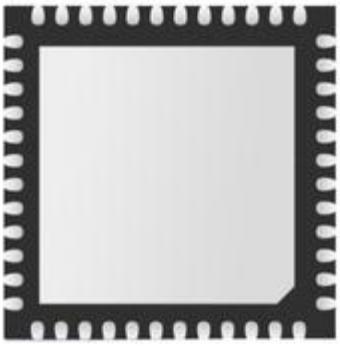
High-Performance Differential Clock Buffer （CTB2310)

Description

California Triangle provides high-performance, low-noise differential clock buffers for communication, radar, measurement, and industrial control applications. These buffers are designed for high-frequency, low-jitter clock/data distribution and level shifting. The input clock can be selected from two differential inputs or one crystal input. The selected input clock is distributed to two sets of outputs, each set containing five differential outputs and one LVCMOS output with sync functionality. The two differential output groups can be independently configured to LVPECL, LVDS, or HCSL levels, or set to output high impedance. The LVCMOS output features a sync enable input control that generates glitch-free clock output during enable or disable operations. Additional jitter is specified at up to 41 fs.

Product view

CTB2310 Front View

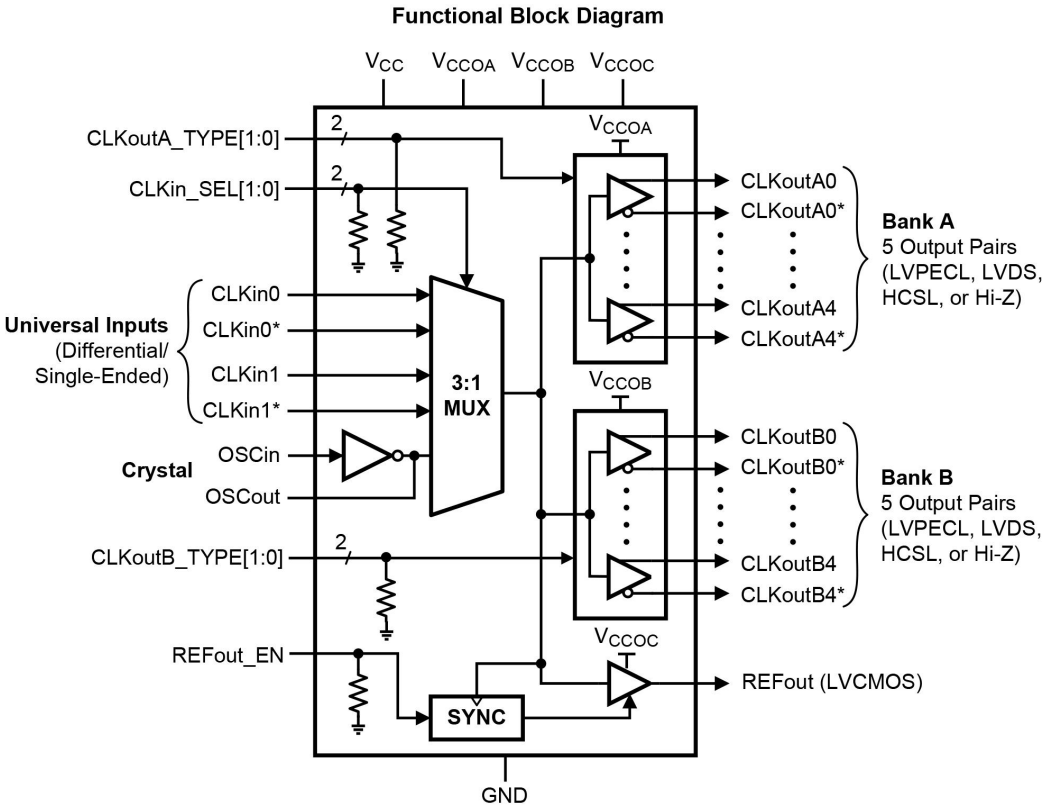


CTB2310 Rear View

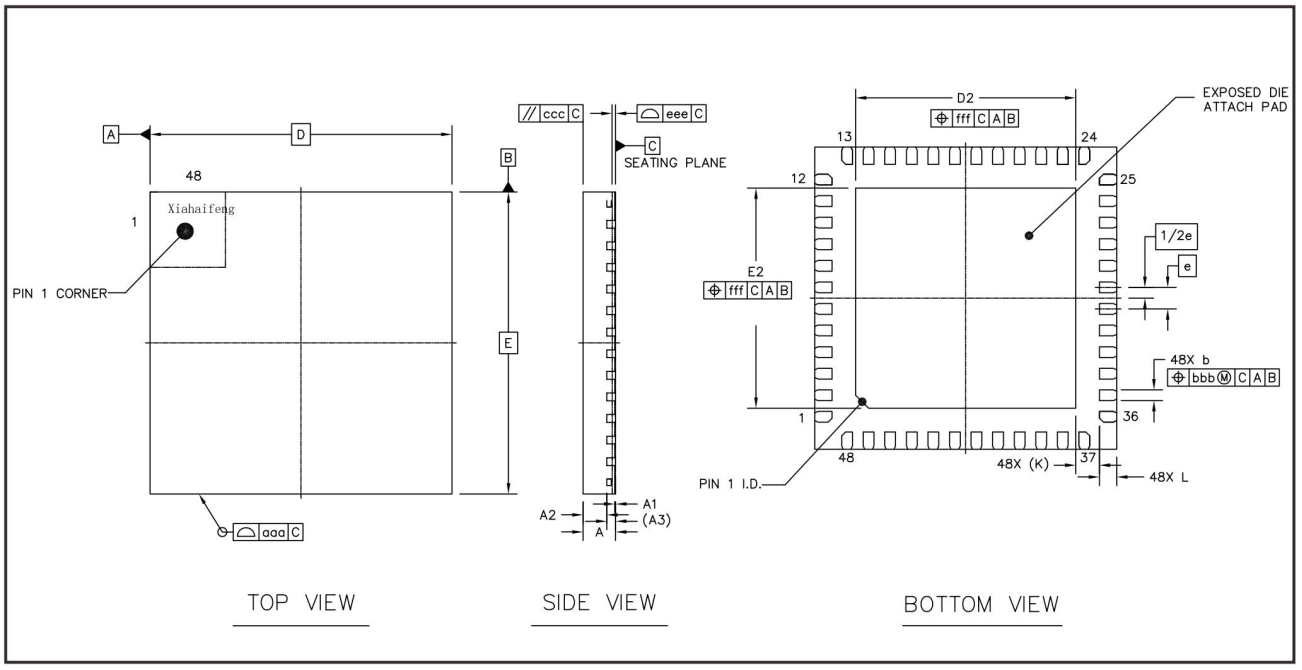
Key Performance Indicators

Model	Frequency Range	Input Level Type	Number of Input Ports	Core Voltage	Output Voltage	Number of Output Ports	Output Level Type	Temperature Range	Packaging
CTB2310	DC~2.1GHz	LVPECL LVDS HCSL SSTL LVCMOS /LVTTL Crystal Oscillator	3	3.3V	2.5V 3.3V	11	LVCMOS LVPECL LVDS HCSL	-40~+85℃	QFN48

Functional Diagram



Packaging Diagram



Packaging Information

		SYMBOL	MIN	NOM	MAX
TOTAL THICKNESS		A	0.7	0.75	0.8
STAND OFF		A1	0	0.02	0.05
MOLD THICKNESS		A2	---	0.55	---
L/F THICKNESS		A3		0.203 REF	
LEAD WIDTH		b	0.2	0.25	0.3
BODY SIZE	X	D		7 BSC	
	Y	E		7 BSC	
LEAD PITCH		e		0.5 BSC	
EP SIZE	X	D2	5	5.1	5.2
	Y	E2	5	5.1	5.2
LEAD LENGTH		L	0.3	0.4	0.5
LEAD TIP TO EXPOSED PAD EDGE		K		0.55 REF	
PACKAGE EDGE TOLERANCE		aaa		0.1	
MOLD FLATNESS		ccc		0.1	
COPLANARITY		eee		0.08	
LEAD OFFSET		bbb		0.1	
EXPOSED PAD OFFSET		fff		0.1	